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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,528	05/12/2004	David R. Stauffer	BUR920030196US1	3527

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EXAMINER
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ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>12 May 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-20</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-6,8-12 and 14-20</u> is/are rejected.

7)☒ Claim(s) <u>7 and 13</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>12 May 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/709,528, filed on 5/12/2004. Claims 1-

20 are pending in this application.

Specification

1.   The abstract of the disclosure is objected to because: the title of the invention

does not belong as part of the abstract; the title of the invention should be removed from

the abstract. Correction is required. See MPEP § 608.01(b).

Claim Objections

2.   Claims 1, 8 and 14 are objected to because of the following informalities: With

respect to the phrases: "generating a core/pin rule" and "generate a core/pin rule", the

intended meaning of the backslash '/' is unclear, and requires clarification. Appropriate

correction is required.

Claim Rejections - 35 USC § 101

3.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

4.   **Claims 14-20 are rejected under 35 U.S.C. 101** because the claimed invention

lacks patentable utility. With respect to claim 14, the claim recites a computer readable

medium which for building an automated datapath system generating tool for a datapat

system. However, the subject matter of the claim fails to explicitly recite the computer

readable medium being executed, or the medium causing a computer to perform the

following steps. Without this explicit recitation, the subject matter of claim 14 does not

provide a useful result or product, and is therefore not considered having patentable

utility because the relationship between the computer and computer-readable medium

is not explicitly recited. Examiner suggests the following amendment to line 3 of claim

14: --code embodied therein, which when executed, causing a computer to build an

automated datapath--. With respect to the limitations of claim 14 lines 8-17, examiner

suggests amending every instance of the phrase: "program code configured to", to the

following: --program code, which when executed, configured to--.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   **Claim 1-6, 8-12 and 14-19 are rejected under 35 U.S.C. 102(b)** as being

anticipated by Choukalos et al. (6,425,109).

7.   With respect to claims 1, 8 and 14, Choukalos teaches a method, system and

computer program product comprising the steps of: defining at least one system

characteristic (pin groups G0, G1 and G2 of Figure 3 ASIC system, also see Col 4, lines

21-45); generating a core/pin rule (i.e. pin configuration rules, see Col 3, lines 49-67) for

the design that defines each core of the design (the elements of Figure 3, considered as

cores, have their structures defined, see Col 4, lines 21-45), each pin of each core and

corresponding pin attributes (pin and pin names are described, Col 4, lines 21-45);

constructing class-type inference rules (NOTE: applicant's examples of class-type

inference rules on page 13 of the specification; Choukalos: a designer defines

relationship between core inputs and outputs [wired-relationship] by writing source code

to define the functionality of the core(s), see Col 3, lines 55-67) for automatically

generating the datapath system (create high-level source by interconnecting cores, i.e.

creating datapath system for ASIC, see Figure 2), each class-type inference rule

executing at least one primitive function (design connectivity is checked against the

physical and logical rules in the PCS, i.e. checking the relationship between input and

output pins, Col 4, lines 12-20; Examiner Notes that, on page 56 of the specification, the

test_class_structure primitive function checks the relationship between the number of

input pins and output pins).

8.   With respect to claims 2, 9 and 15, Choukalos teaches all the elements of claims

1, 8 and 14, from which the claims depend respectively. Choukalos teaches: defining a

set of cores to be used in the datapath system (user selects the core chiplets that the

user desires to be integrated into the core, Col 4, lines 2-5; also see Col 3, lines 30-34

wherein it is stated that a chiplet is merely a core of relatively low complexity); and

defining each stage of each core (see Col 4, Table 1; also see discussion of Pin

Configuration Structures, Col 3, lines 55-67); and establishing a link order name for

each stage (see Col 4, Table 1: LINK_NAME and Link_ORDER). With respect to claim

9 alone, Choukalos teaches: means for identifying any global attributes for a plurality of

pins (creating a global signal name out of LINK_NAME, Col 4, line 38).

9.   With respect to claims 3 and 16, Choukalos teaches all the elements of claims 2

and 15, from which the claims depend respectively. Choukalos teaches: identifying any

global attributes for a plurality of pins (creating a global signal name out of LINK_NAME,

Col 4, line 38).

10.   With respect to claims 4, 10 and 17, Choukalos teaches all the elements of

claims 1, 8 and 14, from which the claims depend respectively. Choukalos teaches:

bundling pins of each stage according to at least one class (see Figure 4, Controller 40

has 3 pins of the same class: ROM_ADDR_0, ROM_ADDR_1, ROM_ADDR_2), each

class indicating a common wiring parameter for the pins (all three ROM_ADDR pins

have same LINK_NAME, see Col 4, lines 35-40), wherein the class is a pin attribute

(the class name may be considered the LINK_NAME itself, wherein the LINK_NAME is

a pin attribute for those pins within the same class); categorizing each class as one of a

plurality of datapath system class-types (LINK_NAMES may become a global signal

name for the entire design, see Col 4, lines 35-40); bundling pins according to at least

one channel identifier (G2 is a channel identifier for the pin group G2, see Figures 3,

#40), wherein the channel identifier is a pin attribute (see the Group_ID attribute in

Table 1 of Figure 4); and generating the core/pin rule that defines each core of the

design (the elements of Figure 3, considered as cores, have their structures defined,

see Col 4, lines 21-45), each pin of each core and corresponding pin attributes.

11.   With respect to claim 5, 11 and 18, Choukalos teaches all the elements of claims

4, 10 and 17, from which the claims depend respectively. Choukalos teaches:

assigning a vector index to each pin within a multiple pin core having more than one pin

with the same class and channel identifier (see the indices 0,1 and 2 of #40 in Figure 3),

wherein the vector index is a pin attribute (see the Group I.D. entry of Table 1 in Col 4, which may have an index as its value, i.e. 0, 1 etc.).

12.   With respect to claims 6, 12 and 19, Choukalos teaches all the elements of claims 4, 10 and 17, from which the claims depend respectively. Choukalos teaches: bundling pins according to at least one global attribute (class names like LINK_NAMES becoming global signal names, Col 4, lines 35-40), each global attribute indicating a common global parameter of the pins.

Allowable Subject Matter

13.   Claims 7, 13 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14.   The following is a statement of reasons for the indication of allowable subject matter: The prior art made of record fails to teach all the limitations of each of claims 7, 13 and 20. Specifically, the prior art made of record fails to teach: establishing a set of primitive functions for use in constructing the class-type inference rules.
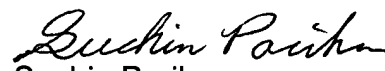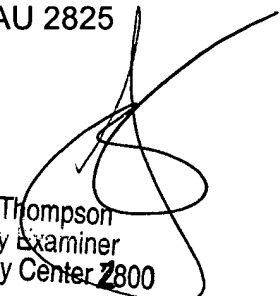
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

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have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

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